AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claim 1 (original): A method for reusing a resource for designing an operational amplifier, comprising the steps of:

preparing different sets of layout information for an operational amplifier comprising a plurality of transistors, said plurality of transistors having their channel widths varied by different factors among said different sets of operational amplifier layout information; and

selecting one of said different sets of operational amplifier layout information and determining the value of a bias current of said operational amplifier so that a required characteristic is satisfied.

Claim 2 (original): The method for reusing a resource for designing an operational amplifier according to claim 1, wherein said operational amplifier has a circuit configuration in which a bias voltage generated by a bias generating circuit is applied to a transistor serving as a current source of said operational amplifier, thereby supplying a current corresponding to a constant multiple of a bias current of said bias generating circuit as a bias current of said operational amplifier,

said method of reusing further comprising a step of previously setting a relation between

the value of the bias current of the operational amplifier represented by said different sets of layout information and the value of the bias current of said bias generating circuit so that a set of operational amplifier layout information can be uniquely selected from said different sets of operational amplifier layout information and the value of the bias current of said bias generating circuit can be uniquely determined on the basis of the value of the bias current of said operational amplifier which satisfies said required characteristic.

Claim 3 (original): The method for reusing a resource for designing an operational amplifier according to claim 2, further comprising a step of previously setting said different factors and the value of the bias current of said bias generating circuit so that the bias current of said operational amplifier continuously varies.

Claim 4 (original): The method for reusing a resource for designing an operational amplifier according to claim 2, further comprising the steps of determining an upper limit of a bias voltage applied to a transistor serving as a current source of said operational amplifier on the basis of an output voltage range, and determining a lower limit of said bias voltage on the basis of cutoff of said transistor serving as a current source.

Claim 5 (original): The method for reusing a resource for designing an operational amplifier according to claim 1, wherein said different factors include three or four different factors.

Claim 6 (original): The method for reusing a resource for designing an operational amplifier according to claim 2, wherein said plurality of transistors further comprise a pair of transistors having a differential configuration and said transistor serving as a current source supplies a current to said pair of transistors.

Claim 7 (original): The method for reusing a resource for designing an operational amplifier according to claim 1, wherein each of said plurality of transistors comprises a field-effect transistor.

Claim 8 (currently amended): An operational amplifier, comprising: a plurality of composite transistors including a composite transistor serving as a current source; a bias generating circuit that applies a bias voltage to said composite transistor serving as a current source; and ~~a~~ an effective channel width varying circuit that varies the effective channel widths of said plurality of composite transistors, thereby realizing a method for reusing a resource for designing an operational amplifier comprising preparing different sets of layout information for an operational amplifier comprising a plurality of composite transistors, said plurality of composite transistors having their effective channel widths varied by different factors among said different sets of operational amplifier layout information, and selecting one of said different sets of operational amplifier layout information and determining the value of a bias current of said operational amplifier so that a required characteristic is satisfied.

Claim 9 (original): The operational amplifier according to claim 8, further comprising a bias voltage adjusting circuit that adjusts the bias voltage generated by said bias generating circuit.

Claim 10 (currently amended): The operational amplifier according to claim 8, wherein said plurality of composite transistors further include a pair of composite transistors having a differential configuration and said composite transistor serving as a current source supplies a current to said pair of composite transistors.

Claim 11 (original): An operational amplifier, comprising:

a plurality of transistors including a transistor serving as a current source;

a bias generating circuit that applies a bias voltage to said transistor serving as a current source; and

a bias voltage adjusting circuit that adjusts the bias voltage generated by said bias generating circuit,

thereby realizing a method for reusing a resource for designing an operational amplifier comprising preparing different sets layout information for an operational amplifier comprising a plurality of transistors, said plurality of transistors having their channel widths varied by different factors among said different sets of operational amplifier layout information, and selecting one of said different sets of operational amplifier layout information and determining the value of a bias current of said operational amplifier so that a required characteristic is satisfied.

Claim 12 (original): The operational amplifier according to claim 11, wherein said plurality of transistors further include a pair of transistors having a differential configuration and said transistor serving as a current source supplies a current to said pair of transistors.

Claim 13 (currently amended): An operational amplifier, comprising:

a plurality of composite transistors including a composite transistor serving as a current source;

a bias generating circuit that applies a bias voltage to said composite transistor serving as a current source; and

~~a~~ an effective channel width varying circuit that varies the effective channel widths of said plurality of composite transistors.

Claim 14 (currently amended): An operational amplifier, comprising:

a plurality of transistors including a transistor serving as a current source;

a bias generating circuit that applies a bias voltage to said transistor serving as a current source; and

a bias voltage adjusting circuit that adjusts the bias voltage generated by said bias generating circuit to change the current flowing through said transistor serving as a current source.

Claim 15 (original): An operational amplifier layout generating apparatus, comprising:

first input means for entering a characteristic required for an operational amplifier;

second input means for entering different sets of layout information for the operational amplifier, said operational amplifier comprising a plurality of transistors, said plurality of transistors having their channel widths varied by different factors among said different sets of operational amplifier layout information;

third input means for entering a relation between the value of a bias current of the operational amplifier represented by said different sets of layout information, and said different factors and the value of a bias current of a bias generating circuit; determining means for determining the bias current of said operational amplifier on the basis of said characteristic entered through said first input means;

selecting means for determining the bias current of said bias generating circuit and selecting one of said different sets of operational amplifier layout information entered through said second input means on the basis of said relation entered through said third input means and the bias current of said operational amplifier determined by said determining means;

executing means for executing a simulation about the operational amplifier using the set of operational amplifier layout information selected by said selecting means; and

output means for outputting the layout information selected by said selecting means when a result of the simulation executed by said executing means satisfies the characteristic entered through said first input means.

Claim 16 (original): An operational amplifier layout generating program for generating a

layout for an operational amplifier, said layout generating program being capable of being read by a computer, said layout generating program causing said computer to execute a process comprising,

accepting an input of a characteristic required for an operational amplifier;

accepting an input of different sets of layout information for the operational amplifier, said operational amplifier comprising a plurality of transistors, said plurality of transistors having their channel widths varied by different factors among said different sets of operational amplifier layout information;

accepting an input of a relation between the value of a bias current of the operational amplifier represented by said different sets of layout information, and said different factors and the value of a bias current of a bias generating circuit;

determining the bias current of said operational amplifier on the basis of said entered characteristic;

determining the bias current of said bias generating circuit and selecting one of said entered different sets of operational amplifier layout information on the basis of said entered relation and said determined bias current of said operational amplifier;

executing a simulation about the operational amplifier using the selected set of operational amplifier layout information; and

outputting the selected operational amplifier layout information when a result of the simulation satisfies said entered characteristic.

Claim 17 (original): An operational amplifier layout generating apparatus, comprising:

a first input device that enters a characteristic required for an operational amplifier;

a second input device that enters different sets of layout information for the operational amplifier, said operational amplifier comprising a plurality of transistors, said plurality of transistors having their channel widths varied by different factors among said different sets of operational amplifier layout information;

a third input device that enters a relation between the value of a bias current of the operational amplifier represented by said different sets of layout information, and said different factors and the value of a bias current of a bias generating circuit;

a processing unit that determines the bias current of said operational amplifier on the basis of said characteristic entered through said first input device, determines the bias current of said bias generating circuit and selects one of said different sets of operational amplifier layout information entered through said second input device on the basis of said relation entered through said third input device and said determined bias current of said operational amplifier, and executes a simulation about the operational amplifier using said selected set of operational amplifier layout information; and

an output device that outputs said selected layout information when a result of the simulation executed by said processing unit satisfies the characteristic entered through said first input device.

Claim 18 (previously presented): The operational amplifier according to claim 14,

wherein said bias voltage adjusting circuit comprises a plurality of switches for adjusting the bias voltage among a plurality of values.